Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of the claims in the application:

Listing of Claims:

Claims 1 – 16 (cancelled).

Claim 17 (currently amended). A multi-layer printed circuit board having at least one prefabricated integrated electronic component embedded therein comprising:

a polymeric circuit board substrate comprising the core of said multi-layer printed circuit board and having a first substrate surface and a second substrate surface;

a first integrated electronic component, where said first integrated electronic component is prefabricated prior to being securely attached in a cavity in said first substrate surface;

a first dielectric layer disposed on said first substrate surface and over said first integrated electronic component;

a metallic layer disposed on said first dielectric layer;

an electrically conductive first via passing through said first dielectric layer in contact with said metallic layer; and

a second dielectric layer disposed over said first via and over said metallic layer,

a second electrically conductive via extending at one location through said first and second dielectric layers and electrically coupled to said first integrated electronic component.

Claim 18 (previously presented). The multi-layer printed circuit board of Claim 17 additionally comprising a first metallic layer disposed on said first substrate surface and a second metallic layer disposed on said second substrate surface.

Claim 19 (previously presented). The multilayer printed circuit board of Claim 17 wherein said circuit board substrate comprises a multi-layer core substrate comprising at least two polymeric layers.

Claim 20 (previously presented). The multilayer printed circuit board of Claim 17 wherein said first via extends from said first substrate surface to said second substrate surface.

Claim 21 (previously presented). The multilayer printed circuit board of Claim 18 wherein said first via extends from said first substrate surface to said second substrate surface.

Claim 22 (previously presented). The multilayer printed circuit board of Claim 18 wherein said first metallic layer is patterned to expose a portion of said first substrate surface, and said cavity is formed in the exposed portion of said first substrate surface.

Claim 23 (previously presented). The multilayer printed circuit board of Claim 18 wherein said second metallic layer is patterned to expose a portion of said second substrate surface.

Claim 24 (original). The multilayer printed circuit board of Claim 23 additionally comprising a second integrated electronic component secured to said exposed portion of said second substrate surface.

Claim 25 (cancelled).

Claim 26 (previously presented). The multilayer printed circuit board of Claim 24 wherein said second integrated electronic component is disposed in a cavity formed in said exposed portion of said second substrate surface.

Claim 27 (previously presented). The multilayer printed circuit board of Claim 18 wherein said first prefabricated integrated electronic component comprises a conductive pad contacting said first metallic layer.

Claim 28 (previously presented). The multilayer printed circuit board of Claim 24 wherein said second integrated electronic component comprises a conductive pad contacting said second metallic layer.

Claim 29 (previously presented). The multilayer printed circuit board of Claim 26 wherein said first prefabricated integrated electronic component comprises a conductive pad contacting said first metallic layer.

Claim 30 (original). The multilayer printed circuit board of Claim 17 additionally comprising at least one metal-lined via extending through said metallic layer and through said first dielectric layer.

Claim 31 (previously presented). The multilayer printed circuit board of Claim 24 additionally comprising at least one metal-lined via extending through said metallic layer and through said first dielectric layer.

Claim 32 (original). The multilayer printed circuit board of Claim 26 additionally comprising at least one metal-lined via extending through said metallic layer and through said first dielectric layer.

Claim 33 (original). The multilayer printed circuit board of Claim 27 additionally comprising at least one metal-lined via extending through said metallic layer and through said first dielectric layer.

Claim 34 (original). The multilayer printed circuit board of Claim 33 additionally comprising a patterned metal layer disposed on said second dielectric layer.

Claim 35 (cancelled).

Claim 36 (previously presented). The multilayer printed circuit board of Claim 17 wherein said first prefabricated integrated electronic component is a capacitor.

Claim 37 (previously presented). The multilayer printed circuit board of Claim 36 wherein said capacitor comprises a petrovskite capacitance material.

Claim 38 (previously presented). The multilayer printed circuit board of Claim 17 wherein said first prefabricated integrated electronic component is fabricated at a temperature higher than the maximum processing temperature of the printed circuit board.

Claim 39 (previously presented). The multilayer printed circuit board of Claim 38 wherein said first prefabricated integrated electronic component is fabricated at a temperature of greater than about 600°C.

Claim 40 (currently amended). A multi-layer printed circuit board comprising:

a polymeric circuit board substrate comprising the core of said multi-layer printed circuit board;

a prefabricated capacitor disposed in a cavity in said substrate, said capacitor having a contact pad;

a first dielectric layer disposed on said substrate and over said capacitor;

a metallic layer disposed on said first dielectric layer;

an electrically conductive first via passing through said first dielectric layer in contact with said contact pad; and

a second dielectric layer disposed over said first via and over said metallic layer,

a second electrically conductive via extending <u>at one location</u> through said first and second dielectric layers and electrically coupled to said capacitor.

Claim 41 (previously presented). The multi-layer printed circuit board of claim 40, comprising a plurality of cavities and a plurality of capacitors.

Claim 42 (previously presented). The multi-layer printed circuit board of claim 40 wherein said capacitor comprises a petrovskite capacitance material.

Claim 43 (previously presented). The multi-layer printed circuit board of claim 40 wherein said capacitor is fabricated at a temperature higher than the maximum processing temperature of the printed circuit board.

Claim 44 (currently amended). A multi-layer printed circuit board comprising:

a polymeric circuit board substrate comprising the core of said multi-layer printed circuit board, said substrate having opposing first and second sides;

a prefabricated electronic component disposed in a cavity formed in said first side of said substrate, said prefabricated electronic component having a contact pad;

a first dielectric layer disposed on said first side of said substrate and over said prefabricated electronic component;

a patterned metallic layer disposed on said first dielectric layer;

an electrically conductive first via passing through said first dielectric layer in contact with said contact pad;

a second dielectric layer disposed over said first via and over said metallic layer;

a second electrically conductive via extending at one location through said first and second dielectric layers;

a third dielectric layer disposed on said second side of said substrate; and

a patterned metallic layer disposed on said third dielectric layer.